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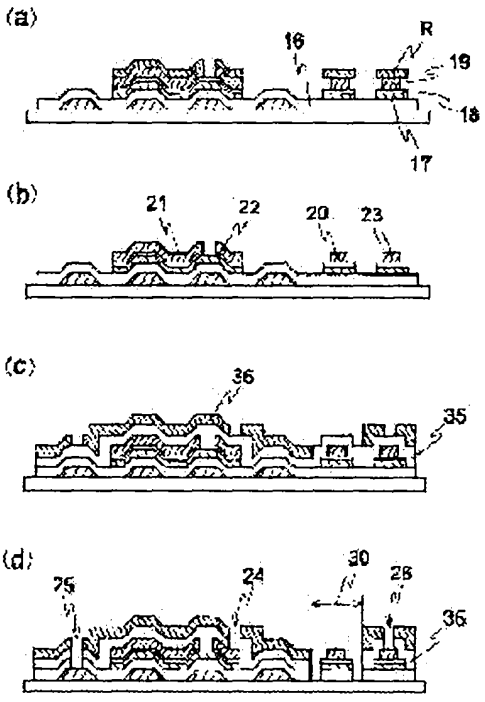
(54) METHOD FOR MANUFACTURING TFT ARRAY SUBSTRATE OF LIQUID CRYSTAL DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To actualize an increase in aperture rate and a decrease in source wire resistance and to prevent source-common capacity from increasing by removing a semiconductor layer which projects from the side of a source wire.

SOLUTION: When a contact hole is formed by removing part of a protection film, the protection film on the source wire, the protection film by the source wire, and the gate insulating film by the source wire are removed at the same time and the part of the exposed semiconductor layer which projects from the side of the source wire is removed by using as a mask a resist pattern for removing part of the protection film and/or the source wire.



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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture method of the TFT array substrate of an active matrix type liquid crystal display especially about the manufacture method of a liquid crystal display.
[0002]
[Description of the Prior Art] A liquid crystal display uses the electro-optics property of liquid crystal, and combines it with a polarizing plate, and it displays by controlling the voltage impressed to liquid crystal, and compared with CRT, a weight is small excellent in portability and is applied to the display of a mobile computer etc. in recent years.
[0003] The active matrix type liquid crystal display which controls voltage which forms switching elements, such as TFT (TFT), in each pixel, and is impressed to liquid crystal especially has the feature of excelling in display grace, as compared with the simple matrix type liquid crystal display, and the development and application are performed briskly.
[0004] The equal circuit of an active matrix type liquid crystal display fundamental to drawing 1 is shown, and the operation is explained. Drawing 1 (b) is drawing which carried out partial expansion of the P section of drawing 1 (a).
[0005] The switching elements 7, such as TFT, the liquid crystal capacity 8, and the auxiliary capacity 9 are formed in the intersection of the gate wiring 1 and the source wiring 2, and the pixel is constituted. A pixel is arranged in the shape of a matrix, and a TFT array substrate is formed.
[0006] If a selection pulse is impressed to gate wiring, all the switching elements connected to this gate wiring will be in an ON state, and the signal currently impressed to the source wiring connected to each switching element will be written in liquid crystal capacity and auxiliary capacity through a switching element. If impression of a selection pulse is completed and gate wiring will be in the state where it does not choose, a switching element will be in an OFF state, and the charge written in the aforementioned liquid crystal capacity and auxiliary capacity will be held until 1 vertical-scanning period passes and a selection pulse is again impressed to the aforementioned gate wiring.
[0007] Usually, an active matrix type liquid crystal display forms switching elements, such as TFT, in one side of two substrates which pinch the layer of liquid crystal and counter, is used as a TFT array substrate, prepares a common electrode in another side, and uses it as an opposite substrate.
[0008] The manufacture method of the TFT array substrate by the Prior art is explained using drawing 2 and drawing 3 , and drawing 4 .
[0009] Drawing 2 is the plan to which the important section of a TFT array substrate was expanded. In drawing 2 , TFT which becomes the intersection of the gate wiring 13 and the source wiring 20 from the gate electrode 12, the source electrode 21, and the drain electrode 22 is formed, and the drain electrode 22 of TFT is connected to the pixel electrode 27. In order to impress a selection pulse from the exterior, the edge of the gate wiring 13 is extended besides the viewing area of a liquid crystal display, and forms the lower pad 15. The lower pad 15 is connected with the up pad 28 through the contact hole 25, and a

selection pulse is inputted from here.
[0010] Although not shown in drawing 2 , similarly, the edge of the source wiring 20 is extended besides the viewing area of a liquid crystal display, and forms the lower pad 23. The lower pad 23 is connected with the up pad 29 through the contact hole 26, and a signal is inputted from here.
[0011] Drawing 3 and drawing 4 are the cross sections explaining the manufacture method of the TFT array substrate of drawing 2 .
[0012] First, on the insulating substrate 11, technique, such as a spatter, is used and the 1st metal layer is formed. The 1st metal layer consists of alloys which make a principal component a metal or these metals, such as Cr, aluminum, and Mo, or these laminatings. Subsequently, photoengraving process is performed using a photoresist etc., a garbage is removed from the 1st metal layer by the etching method etc., and the gate electrode 12, the gate wiring 13, the common wiring 14, and the lower pad 15 are formed. This state is drawing 3 (a).
[0013] Next the insulator layer (gate insulator layer) 16 which consists of SiNx, SiO2, etc. It forms by various CVD, such as plasma CVD, the spatter, vacuum evaporationo, the applying method, etc. Furthermore, the a-Si:H layer (1st semiconductor layer) 17, Lynn, antimony, The semiconductor layers (an impurity semiconductor layer, 2nd semiconductor layer) 18 which doped impurities, such as boron, such as an n+a-Si:H film and a micro crystal n+Si layer, are formed by the plasma CVD method, the spatter, etc. Furthermore, the 2nd metal layer 19 is formed using technique, such as a spatter. The 2nd metal layer consists of alloys which make a principal component a metal or these metals, such as Cr, aluminum, and Mo, or these laminatings.
[0014] Subsequently, Photoresist R is applied and the resist pattern which consists of a field C which removed the field A where the thickness of Photoresist R is thick, the field B where the thickness of Photoresist R is thin, and Photoresist R with a photo-engraving process etc. is formed. This state is drawing 3 (b).
[0015] Next, this resist pattern is used and the 2nd metal layer 19 is etched. The 2nd metal layer 19 of the field C without Photoresist R is removed alternatively. This state is drawing 3 (c).
[0016] Then, the photoresist R of Field B is removed. At this time, since thickness is thick, the photoresist R of Field A is left behind, without being removed. This state is drawing 3 (d).
[0017] Next the photoresist R which remained in Field A is used, first, the semiconductor layers 18 and 17 are etched, the semiconductor layers 18 and 17 of Field C are removed, the 2nd metal layer 19 is etched after that, and the 2nd metal layer 19 of Field B is removed. This state is drawing 3 (e) and drawing 4 (a).
[0018] Furthermore, etching removes the semiconductor layer 18 of Field B, and Photoresist R is removed altogether after that. This state is drawing 4 (b). On the substrate, the source wiring 20, the source electrode 21, the drain electrode 22, and the lower pad 23 are formed.
[0019] Then, after forming a protective coat 35 on the whole surface, photoengraving process is performed using a photoresist etc. and contact holes 24, 25, and 26 are formed by the etching method etc. This state is drawing 4 (c).
[0020] Finally, ITO (Indium Tin Oxide) is formed on the whole surface, photoengraving process is performed using a photoresist etc., by the etching method etc., a garbage is removed and the ITO pixel electrode 27 and the up pads 28 and 29 are formed. This state is drawing 4 (d).
[0021]
[Problem(s) to be Solved by the Invention] According to the manufacture method explained above, since a TFT array substrate can be manufactured by a total of four photoengraving process, i.e., the photo mask of four sheets, shortening of a process and reduction of cost are possible.
[0022] In this manufacturing method, however, the source wiring 20, the source electrode 21, the drain electrode 22, and the lower pad 23, The semiconductor layer 18 and the semiconductor layer 17 which are located in these lower parts are formed using the same photoresist R. by moreover, difference of the etching technique and etching conditions the -- two -- a metal -- a layer -- 19 -- etching -- the time -- wiring -- becoming thin -- an amount (the amount of side etch) -- a semiconductor -- a layer -- 18 -- and -- a semiconductor -- a layer -- 17 -- side etch -- an amount -- being large -- things -- from -- drawing 4 -

- (-- a --) - (-- d --) -- seeing -- having -- as -- It becomes the configuration which the semiconductor layer 18 and the semiconductor layer 17 protruded beside the source wiring 20.
[0023] Generally, in the case of Cr, aluminum, Mo, etc., the material of the source wiring 20 (2nd metal layer 19) of the amount of side etch is about 0.5-1.0 micrometers at one side. On the other hand, the amount of side etch of the semiconductor layer 18 and the semiconductor layer 17 is about 0 micrometer. Therefore, when source wiring width of face in the photo mask used for photoengraving process is set to 10 micrometers, the width of face of the source wiring actually formed is set to 8-9 micrometers, and the semiconductor layer 18 and the semiconductor layer 17 will disturb about 1-2 micrometers, and will be formed.
[0024] It is desirable to enable the display of high brightness, and to enlarge the numerical aperture of a TFT array substrate as much as possible, in order to obtain the liquid crystal display excellent in display grace. Moreover, in order to prevent delay of the signal impressed to the source wiring 20 and to prevent deterioration of display grace, such as brightness nonuniformity, as for resistance of the source wiring 20, it is desirable to make it small as much as possible.
[0025] Improvement in a numerical aperture can be aimed at without making small width of face of the source wiring 20, if the flash of the semiconductor layer 18 and the semiconductor layer 17 is removable (i.e., without it increasing resistance of the source wiring 20). Moreover, if it is the same numerical aperture, width of face of the source wiring 20 can be enlarged more, and low resistance-ization of the source wiring 20 can be achieved.
[0026] Furthermore, the overflowing semiconductor layer 18 and the overflowing semiconductor layer 17 form capacity between the common electrodes of an opposite substrate, and the problem that the capacity between source-common increases also has them.
[0027] In the manufacture method of the TFT array substrate by the photo mask of four sheets especially mentioned above, the 2nd metal layer 19 (source wiring 20) will be exposed to etching of multiple times (see drawing 3 (c) and drawing 4 (a)).
[0028] For this reason, the difference with the amount of side etch of the amount of side etch of the source wiring 20, the semiconductor layer 18, and the semiconductor layer 17 will become still larger, for example, the width of face of the source wiring actually formed when the source wiring width of face in a photo mask is 10 micrometers is set to about 6-7 micrometers, and the semiconductor layer 18 and the semiconductor layer 17 will disturb about 3-4 micrometers, and will be formed.
[0029] Therefore, the manufacture method that the semiconductor layer 18 and the semiconductor layer 17 which problems, such as decline in a numerical aperture, resistance increase of source wiring, or increase of the capacity between source-common, became still larger, and were protruded were removable was desired strongly.
[0030] Then, this invention aims at removing the semiconductor layer which disturbed beside source wiring in the manufacturing process of the TFT array of an active matrix type liquid crystal display.
[0031]
[Means for Solving the Problem] In case this invention forms a protective coat after forming gate wiring, source wiring, a TFT element, etc., removes a part of this protective coat and forms a contact hole, it removes simultaneously the protective coat on source wiring, the protective coat beside source wiring, and the gate insulator layer beside source wiring, and exposes the semiconductor layer under source wiring and source wiring.
[0032] Furthermore, the resist pattern for removing a part of protective coat for the portion protruded beside source wiring among the exposed semiconductor layers and/or source wiring are removed as a mask.
[0033] Or the protective coat after removing a part for the portion protruded beside source wiring among the exposed semiconductor layers, and/or source wiring are removed as a mask.
[0034] With the gestalt of another operation of this invention, a protective coat removes source wiring for the portion which was not formed but has been protruded beside source wiring among the semiconductors under the exposed source wiring as a mask after forming gate wiring, source wiring, a TFT element, etc.

[0035] With the gestalt of still more nearly another operation of this invention, when removing a part of protective coat and forming a contact hole by leaving a semiconductor layer beside source wiring at the time of source wiring formation, only the protective coat a source wiring top and beside source wiring is removed, and the gate insulator layer beside source wiring was made not to be removed.
[0036] Furthermore, the resist pattern for removing a part of protective coat for the portion protruded beside source wiring among the semiconductor layers which the protective coat was removed and were exposed, and/or source wiring are removed as a mask.
[0037] Or the protective coat after removing a part for the portion protruded beside source wiring among the semiconductor layers which the protective coat was removed and were exposed, and/or source wiring are removed as a mask.
[0038] In case some ITO films are alternatively removed in this invention, it is good as for a method of a wrap in source wiring by the ITO film by leaving without removing the ITO film on source wiring.
[0039]
[Embodiments of the Invention] Hereafter, the gestalt of operation of this invention is explained using drawing.
[0040] The gestalt of operation of the 1st of gestalt 1 this invention of operation is explained using drawing 5 , drawing 6 , and drawing 7 . Drawing 5 , drawing 6 , and drawing 7 are the cross sections which illustrated the TFT array substrate in which reverse stagger type TFT was prepared, and explained the manufacture method.
[0041] The manufacture method of the TFT array substrate by the gestalt of operation of the 1st of this invention consists of the following processes.
[0042] (1) First, form the 1st metal layer on the insulating substrate 11, subsequently, perform photoengraving process using a photoresist etc., remove a garbage from the 1st metal layer by the etching method etc., and form the gate electrode 12, the gate wiring 13, the common wiring 14, and the lower pad 15 (drawing 5 (a)).
[0043] (2) Next, form on a substrate four layers, the gate insulator layer 16 and the a-Si layer (the amorphous-semiconductor film, 1st semiconductor layer) 17 which consist of SiNx, SiO2, etc., the n+a-Si layer (an amorphous impurity semiconductor film, 2nd semiconductor layer) 18, and the 2nd metal layer 19, so that these gates electrode 12, the gate wiring 13, the common wiring 14, and the pad layer 15 may be covered.
[0044] (3) Form the resist pattern with which the thickness of Photoresist R consists Photoresist R of a field C which removed the thick field A, the thin field B, and Photoresist R after an application using a photo mask.
[0045] The thick field A of Photoresist R the field for leaving the 2nd metal layer 19 as a source electrode, a drain electrode, source wiring, or drain wiring, and the field C which removed Photoresist R The field for **********ing and removing the 2nd metal layer 19, the 2nd semiconductor layer 18, and the 1st semiconductor layer 17 at least The 2nd metal layer 19 and the 2nd semiconductor layer 18 are removed, and the thin field B of Photoresist R is equivalent to the field used as the channel section 38 of TFT, respectively (drawing 5 (b)).
[0046] Only the channel section 38 of TFT is made into Field B with the gestalt of this operation. Although only the TFT channel section 38 does not need to be Field B, in the gestalt of this operation, only the portion which serves as the source wiring 20 at least behind, and its near are characterized by not considering as Field B.
[0047] (4) Next, etching etc. removes the 2nd metal layer 19 of C field first (drawing 5 (c)).
[0048] (5) Remove the photoresist R of Field B after that. At this time, since thickness is thick, the photoresist R of Field A is left behind, without being removed (drawing 5 (d)).
[0049] (6) Etching etc. removes the semiconductor layers 18 and 17 of Field C after that (drawing 5 (e)).
[0050] (7) The 2nd metal layer 19 of Field B is removed further (drawing 6 (a)).
[0051] (8) Next, remove the 2nd semiconductor layer 18 of Field B, and remove Photoresist R altogether after that (drawing 6 (b)).

[0052] the process so far is the same as that of what is depended on a Prior art, and as already stated, the source wiring 20 which consists of a metal layer 19 which is the 2nd is in the state where the semiconductor layer 18 and the semiconductor layer 17 overflowed beside the source wiring 20 since the amount of side etch was large compared with the semiconductor layer 18 and the semiconductor layer 17

[0053] (9) Apply a photoresist and form the resist pattern 36 using a photo mask, after forming a protective coat 35 all over the front-face top of the TFT array substrate of this state (drawing 6 (c)).

[0054] Although this resist pattern 36 is for removing a part of protective coat 35 at the following process, and forming contact holes 24, 25, and 26, let it be the pattern from which the protective coat 35 of the field 30 of the source wiring 20 top and its near is also removed simultaneously.

[0055] (10) Using this resist pattern 36, etch a protective coat 35 and form the contact hole 26 for connecting electrically the contact hole 25, the lower pad 23, and the up pad 29 for connecting electrically the contact hole 24, the lower pad 15, and the up pad 28 for connecting electrically the drain electrode 22 and the ITO pixel electrode 27. At this time, as already stated, the protective coat 35 of the field 30 of the source wiring 20 top and its near is removed, and the gate insulator layer 16 of a field 30 is also removed simultaneously (drawing 6 (d)).

[0056] (11) Next perform etching which used the resist pattern 36 and the source wiring 20 as a mask, remove the semiconductor layers 18 and 17 protruded beside the source wiring 20, and remove the resist pattern 36 after that (drawing 7 (a)).

[0057] At this time, a resist pattern may be removed first and you may ********** the protruded semiconductor layers 18 and 17 by using a protective coat 35 and source wiring 20 as a mask.

[0058] Moreover, in case the 2nd metal layer 19 which forms the source wiring 20 **********s the protruded semiconductor layers 18 and 17, the material into which it does not ********** simultaneously, for example, Cr etc., comes out, and it has a certain need.

[0059] (12) Form the ITO pixel electrode 27 and the up pads 28 and 29 by performing photoengraving process using a photoresist etc. and performing patterning which removes the garbage of this ITO film by the etching method etc. after forming an ITO film on the whole surface after that (drawing 7 (b)).

[0060] According to the gestalt of this operation, the semiconductor layer 18 and the semiconductor layer 17 which could manufacture the TFT array substrate by the a total of four same photoengraving process as the conventional manufacture method, i.e., the photo mask of four sheets, and were protruded beside source wiring are removable as explained above.

[0061] Therefore, without causing increase of the time and cost which manufacture takes, low resistance-ization of the improvement in the numerical aperture of a TFT array substrate and source wiring can be achieved, and the problem of increase of the capacity between source-common can also be solved.

[0062] The gestalt of operation of the 2nd of gestalt 2 this invention of operation is explained using drawing 8 .

[0063] The gestalt of this operation is characterized by covering the source wiring 20 with the ITO film 37.

[0064] In the gestalt 1 of operation, if drawing 7 (b) is seen, the source wiring 20 will be exposed so that clearly. Therefore, liquid crystal and material without reactivity needed to be chosen as a material of the source wiring 20 19, i.e., the 2nd metal layer.

[0065] Then, with the gestalt of this operation, when performing patterning of an ITO film, the wrap ITO film 37 was formed for the semiconductor layers 17 and 18 located in the lower layer of the source wiring 20 and the source wiring 20 by leaving the ITO film on the source wiring 20.

[0066] Since the ITO film 37 is covered with the source electrode 20, the degree of material option of the source wiring 20 (2nd metal layer 19) increases. Furthermore, since both the source wiring 20 and the ITO film 37 function as source wiring, resistance of source wiring can be reduced. Moreover, if the source wiring 20 should be disconnected, in order to play a role with the redundant ITO film 37, reliability also improves.

[0067] The gestalt of operation of the 3rd of gestalt 3 this invention of operation is explained using

drawing 9 , drawing 10 , and drawing 11 . Drawing 9 , drawing 10 , and drawing 11 are the cross sections which illustrated the TFT array substrate in which reverse stagger type TFT was prepared, and explained the manufacture method.
[0068] With the gestalt 1 of operation, if drawing 7 (b) is seen, in the field 30 near the source wiring 20, the gate insulator layer 16 is also removed so that clearly. Therefore, when the source wiring 20 and the common wiring 14 adjoin and are formed, there is a possibility that the short-circuit between both wiring may occur. Then, it was made to leave in the about 20 source wiring field 30 with the gestalt of this operation, without removing the gate insulator layer 16.
[0069] The process is explained below.
[0070] (1) first, on the insulating substrate 11, form the 1st metal layer, carry out patterning of this metal layer that is the 1st using photoengraving-process technology, and form the gate electrode 12, the gate wiring 13, the common wiring 14, and the lower pad 15 (drawing 9 (a))
[0071] (2) Next, form four layers, the gate insulator layer 16, the 1st semiconductor layer 17, the 2nd semiconductor layer 18, and the 2nd metal layer 19, on a substrate so that these gates electrode 12, the gate wiring 13, the common wiring 14, and the pad layer 15 may be covered.
[0072] (3) Form the resist pattern with which the thickness of Photoresist R consists Photoresist R of a field C which removed the thick field A (A1), the thin field B (B1), and Photoresist R after an application using a photo mask.
[0073] In the gestalt 1 of operation, although Field B was only the channel section of TFT, in the gestalt of this operation, the thin field B1 of Photoresist R is formed also near the field A1 which serves as source wiring behind (drawing 9 (b)).
[0074] (4) Next, etching etc. removes the 2nd metal layer 19 of C field first (drawing 9 (c)).
[0075] (5) Next, the photoresist R of Field A (A1) removes the photoresist R of Field B (B1), leaving (drawing 9 (d)).
[0076] (6) Etching etc. removes the semiconductor layers 18 and 17 of Field C after that (drawing 9 (e)).
[0077] (7) The 2nd metal layer 19 of Field B (B<SUB> 1) is removed further (drawing 10 (a)).
[0078] (8) Next, remove the 2nd semiconductor layer 18 of Field B (B1), and remove Photoresist R altogether after that (drawing 10 (b)).
[0079] As already stated, the source wiring 20 which consists of the 2nd metal layer 19 is in the state where the 2nd semiconductor layer 18 overflowed beside the source wiring 20 since the amount of side etch was large compared with the 2nd semiconductor layer 18.
[0080] (9) Apply a photoresist, perform photoengraving process using a photo mask, and form the resist pattern 36, after forming a protective coat 35 all over the front-face top of the TFT array substrate of this state (drawing 10 (c)).
[0081] Although this resist pattern 36 is for removing a part of protective coat 35 at the following process, and forming contact holes 24, 25, and 26, let it be the pattern from which the protective coat 35 of the field 30 of the source wiring 20 top and its near is also removed simultaneously.
[0082] (10) Although a protective coat 35 is etched and contact holes 24, 25, and 26 are formed using this resist pattern 36, as already stated, the protective coat 35 of the field 30 of the source wiring 20 top and near is also removed (drawing 10 (d)).
[0083] (11) Next, etch as a mask using the resist pattern 36 and the source wiring 20, remove the semiconductor layer 18 protruded into the lower layer of the source wiring 20, and the about 20 source wiring semiconductor layer 17, and remove a resist pattern after that (drawing 11 (a)).
[0084] At this time, a resist pattern may be removed first and you may ********** the protruded semiconductor layer 18 and the semiconductor layer 17 by using a protective coat 35 and source wiring 20 as a mask.
[0085] Moreover, in case the 2nd metal layer 19 which forms the source wiring 20 **********s the semiconductor layer 18 and the semiconductor layer 17, the material into which it does not ********** simultaneously, for example, Cr etc., comes out, and it has a certain need.
[0086] (12) Form the ITO pixel electrode 27 and the up pads 28 and 29 by carrying out patterning using

photoengraving-process technology after forming an ITO film on the whole surface after that (drawing 11 (b)).
[0087] In order to remain according to the gestalt of this operation, without removing the about 20 source wiring gate insulator layer 16 as explained above, a possibility that the short-circuit between the source wiring 20 and the common wiring 14 may occur disappears.
[0088] Although the source wiring 20 is exposed with the gestalt of this operation, of course, it is possible for an ITO film to cover the source wiring 20 as well as the gestalt 2 of operation.
[0089] The gestalt of operation of the 4th of gestalt 4 this invention of operation is explained using drawing 12 and drawing 13 . Drawing 12 and drawing 13 are the cross sections which illustrated the TFT array substrate in which reverse stagger type TFT was prepared, and explained the manufacture method.
[0090] The gestalt of this operation differs from the gestalt 1 of operation in that the protective coat 35 was omitted.
[0091] The process is explained below.
[0092] (1) first, on the insulating substrate 11, form the 1st metal layer, carry out patterning of this metal layer that is the 1st using photoengraving-process technology, and form the gate electrode 12, the gate wiring 13, the common wiring 14, and the lower pad 15 (drawing 12 (a))
[0093] (2) Next, form four layers, the gate insulator layer 16, the 1st semiconductor layer 17, the 2nd semiconductor layer 18, and the 2nd metal layer 19, on a substrate so that these gates electrode 12, the gate wiring 13, the common wiring 14, and the pad layer 15 may be covered.
[0094] (3) Form the resist pattern with which the thickness of Photoresist R consists Photoresist R of a field C which removed the thick field A, the thin field B, and Photoresist R after an application using a photo mask (drawing 12 (b)).
[0095] (4) Next, etching etc. removes the 2nd metal layer 19 of C field first (drawing 12 (c)).
[0096] (5) Next, the photoresist R of Field A removes the photoresist R of Field B, leaving (drawing 12 (d)).
[0097] (6) Etching etc. removes the semiconductor layers 18 and 17 of Field C after that (drawing 12 (e)).
[0098] (7) The 2nd metal layer 19 of Field B is removed further (drawing 13 (a)).
[0099] (8) Next, remove the 2nd semiconductor layer 18 of Field B, and remove Photoresist R altogether after that (drawing 13 (b)).
[0100] The manufacturing process so far is the same as that of the gestalt 1 of operation, and is in the state where the semiconductor layer 18 and the semiconductor layer 17 overflowed beside the source wiring 20, as [stated / already].
[0101] (9) Apply a photoresist to the front face of the TFT array substrate of this state, form a resist pattern using a photo mask, and form a contact hole in the gate insulator layer 16 on the lower pad 15. Furthermore, etching which used source wiring 20 as the mask removes the semiconductor layer 18 and the half-conductor-layer layer 17 which have been protruded into the lower layer of the source wiring 20 (drawing 13 (c)).
[0102] (10) Form the ITO pixel electrode 27 and the up pads 28 and 29 by carrying out patterning using photoengraving-process technology after forming an ITO film on the whole surface after that. With the gestalt of this operation, the ITO pixel electrode 27, the drain electrode 22, the up pad layer 29, and the lower pad 23 are directly in contact without a contact hole (drawing 13 (d)).
[0103] In the gestalt 1 of operation, in order to remove the semiconductor layer 18 and the semiconductor layer 17 which were protruded beside the source wiring 20, the about 20 source wiring protective coat 35 is removed, and the about 20 source wiring gate insulator layer 16 is also simultaneously removed at this time (drawing 6 (d)). Therefore, when the source wiring 20 and the common wiring 14 adjoin and are formed, there is a possibility that the short-circuit between both wiring may occur.
[0104] According to the gestalt of this operation, since it is not necessary to remove a protective coat 35, the about 20 source wiring gate insulator layer 16 is not removed. Therefore, even when the source

wiring 20 and the common wiring 14 adjoin and are formed, there is no possibility that the short-circuit between both wiring may occur.
[0105] Although the source wiring 20 is exposed with the gestalt of this operation, of course, it is possible for an ITO film to cover the source wiring 20 as well as the gestalt 2 of operation.
[0106] Since the semiconductor layer 18 and the semiconductor layer 17 which could produce the TFT array substrate in a low cost and a short time more, and were protruded beside the source wiring 20 since the protective coat 35 was omitted are removable according to the gestalt of this operation, low resistance-ization of the improvement in a numerical aperture and source wiring can be achieved, and the problem of increase of the capacity between source-common can also be solved.
[0107] The gestalt of operation of the 5th of gestalt 5 this invention of operation is explained using drawing 14 . Drawing 14 is a cross section which illustrates the TFT array substrate in which reverse stagger type TFT was prepared, and explains the manufacture method.
[0108] With the gestalt 4 of operation mentioned above, the TFT array substrate is manufactured by the photo mask of a total of four sheets, i.e., 4 times of photoengraving-process processes. According to the gestalt of this operation, it is possible to manufacture a TFT array substrate by the photo mask of three sheets, i.e., 3 times of photoengraving-process processes.
[0109] In the gestalt 4 of operation, in the process shown in drawing 13 (c), the photoresist was applied to the front face of a TFT array substrate, the resist pattern was formed using the photo mask, and the contact hole was formed in the gate insulator layer 16 on the lower pad 15.
[0110] Then, the ITO pixel electrode 27 and the up pads 28 and 29 are formed by forming an ITO film on the whole surface and carrying out patterning using photoengraving-process technology. Therefore, the lower pad 15 and the up pad 28 are electrically connected through the contact hole.
[0111] With the gestalt of this operation, before forming an ITO film, the gate insulator layer 16 on the lower pad 15 is removed, without using a photo mask (drawing 14 (a)). Removal is performed in the circumference exposure process which exposes the photoresist for a periphery of a TFT array substrate without a mask by also making the photoresist on the lower pad 15 expose, removing, and removing the gate insulator layer 16 on the exposed lower pad 15 according to the continuing etching process. Then, the ITO pixel electrode 27 and the up pads 28 and 29 are formed by forming an ITO film on the whole surface and carrying out patterning using photoengraving-process technology (drawing 14 (b)). In this case, the lower pad 15 and the up pad 28 contact directly, and are connected electrically.
[0112] Since the photoengraving-process process for forming a contact hole in the gate insulator layer 16 becomes unnecessary, it becomes possible to produce a TFT array substrate at 3 times of photoengraving-process processes, i.e., the photo mask of three sheets, and reduction of the further cost is possible.
[0113] Of course, since the semiconductor layer 18 and the semiconductor layer 17 which were protruded beside the source wiring 20 are removable like the gestalt of other operations, low resistance-ization of the improvement in a numerical aperture and source wiring can be achieved, and the problem of increase of the capacity between source-common can also be solved.
[0114] Although the source wiring 20 is exposed with the gestalt of this operation, of course, it is possible for an ITO film to cover the source wiring 20 as well as the gestalt 2 of operation.
[0115]
[Effect of the Invention] It is the manufacturing process which used the photo mask of four sheets of a Prior art and the same number, or the photo mask of three sheets fewer than a Prior art by applying the manufacture method of this invention. It becomes possible to remove the semiconductor layer protruded beside source wiring, and decline in a numerical aperture, increase of source wiring resistance, and increase of source-common interelectrode capacity can be prevented, and it becomes cheaply possible about a quality liquid crystal display to manufacture for a short time.
[0116] Furthermore, by covering source wiring by the ITO film, the reaction of source wiring and liquid crystal can be prevented and the degree of material option of source wiring can be raised. Moreover, since an ITO film also functions as source wiring in addition to original source wiring, while being able to achieve much more low resistance-ization of source wiring and obtaining a quality liquid crystal

display, the possibility of an open circuit of source wiring decreases and reliability improves.

[Translation done.]

* NOTICES *

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PRIOR ART

[Description of the Prior Art] A liquid crystal display uses the electro-optics property of liquid crystal, and combines it with a polarizing plate, and it displays by controlling the voltage impressed to liquid crystal, and compared with CRT, a weight is small excellent in portability and is applied to the display of a mobile computer etc. in recent years.
[0003] The active matrix type liquid crystal display which controls voltage which forms switching elements, such as TFT (TFT), in each pixel, and is impressed to liquid crystal especially has the feature of excelling in display grace, as compared with the simple matrix type liquid crystal display, and the development and application are performed briskly.
[0004] The equal circuit of an active matrix type liquid crystal display fundamental to drawing 1 is shown, and the operation is explained. Drawing 1 (b) is drawing which carried out partial expansion of the P section of drawing 1 (a).
[0005] The switching elements 7, such as TFT, the liquid crystal capacity 8, and the auxiliary capacity 9 are formed in the intersection of the gate wiring 1 and the source wiring 2, and the pixel is constituted. A pixel is arranged in the shape of a matrix, and a TFT array substrate is formed.
[0006] If a selection pulse is impressed to gate wiring, all the switching elements connected to this gate wiring will be in an ON state, and the signal currently impressed to the source wiring connected to each switching element will be written in liquid crystal capacity and auxiliary capacity through a switching element. If impression of a selection pulse is completed and gate wiring will be in the state where it does not choose, a switching element will be in an OFF state, and the charge written in the aforementioned liquid crystal capacity and auxiliary capacity will be held until 1 vertical-scanning period passes and a selection pulse is again impressed to the aforementioned gate wiring.
[0007] Usually, an active matrix type liquid crystal display forms switching elements, such as TFT, in one side of two substrates which pinch the layer of liquid crystal and counter, is used as a TFT array substrate, prepares a common electrode in another side, and uses it as an opposite substrate.
[0008] The manufacture method of the TFT array substrate by the Prior art is explained using drawing 2 and drawing 3 , and drawing 4 .
[0009] Drawing 2 is the plan to which the important section of a TFT array substrate was expanded. In drawing 2 , TFT which becomes the intersection of the gate wiring 13 and the source wiring 20 from the gate electrode 12, the source electrode 21, and the drain electrode 22 is formed, and the drain electrode 22 of TFT is connected to the pixel electrode 27. In order to impress a selection pulse from the exterior, the edge of the gate wiring 13 is extended besides the viewing area of a liquid crystal display, and forms the lower pad 15. The lower pad 15 is connected with the up pad 28 through the contact hole 25, and a selection pulse is inputted from here.
[0010] Although not shown in drawing 2 , similarly, the edge of the source wiring 20 is extended besides the viewing area of a liquid crystal display, and forms the lower pad 23. The lower pad 23 is connected with the up pad 29 through the contact hole 26, and a signal is inputted from here.
[0011] Drawing 3 and drawing 4 are the cross sections explaining the manufacture method of the TFT array substrate of drawing 2 .

[0012] First, on the insulating substrate 11, technique, such as a spatter, is used and the 1st metal layer is formed. The 1st metal layer consists of alloys which make a principal component a metal or these metals, such as Cr, aluminum, and Mo, or these laminatings. Subsequently, photoengraving process is performed using a photoresist etc., a garbage is removed from the 1st metal layer by the etching method etc., and the gate electrode 12, the gate wiring 13, the common wiring 14, and the lower pad 15 are formed. This state is drawing 3 (a).
[0013] Next the insulator layer (gate insulator layer) 16 which consists of SiNx, SiO2, etc. It forms by various CVD, such as plasma CVD, the spatter, vacuum evaporationo, the applying method, etc. Furthermore, the a-Si:H layer (1st semiconductor layer) 17, Lynn, antimony, The semiconductor layers (an impurity semiconductor layer, 2nd semiconductor layer) 18 which doped impurities, such as boron, such as an n+a-Si:H film and a micro crystal n+Si layer, are formed by the plasma CVD method, the spatter, etc. Furthermore, the 2nd metal layer 19 is formed using technique, such as a spatter. The 2nd metal layer consists of alloys which make a principal component a metal or these metals, such as Cr, aluminum, and Mo, or these laminatings.
[0014] Subsequently, Photoresist R is applied and the resist pattern which consists of a field C which removed the field A where the thickness of Photoresist R is thick, the field B where the thickness of Photoresist R is thin, and Photoresist R with a photo-engraving process etc. is formed. This state is drawing 3 (b).
[0015] Next, this resist pattern is used and the 2nd metal layer 19 is etched. The 2nd metal layer 19 of the field C without Photoresist R is removed alternatively. This state is drawing 3 (c).
[0016] Then, the photoresist R of Field B is removed. At this time, since thickness is thick, the photoresist R of Field A is left behind, without being removed. This state is drawing 3 (d).
[0017] Next the photoresist R which remained in Field A is used, first, the semiconductor layers 18 and 17 are etched, the semiconductor layers 18 and 17 of Field C are removed, the 2nd metal layer 19 is etched after that, and the 2nd metal layer 19 of Field B is removed. This state is drawing 3 (e) and drawing 4 (a).
[0018] Furthermore, etching removes the semiconductor layer 18 of Field B, and Photoresist R is removed altogether after that. This state is drawing 4 (b). On the substrate, the source wiring 20, the source electrode 21, the drain electrode 22, and the lower pad 23 are formed.
[0019] Then, after forming a protective coat 35 on the whole surface, photoengraving process is performed using a photoresist etc. and contact holes 24, 25, and 26 are formed by the etching method etc. This state is drawing 4 (c).
[0020] Finally, ITO (Indium Tin Oxide) is formed on the whole surface, photoengraving process is performed using a photoresist etc., by the etching method etc., a garbage is removed and the ITO pixel electrode 27 and the up pads 28 and 29 are formed. This state is drawing 4 (d).

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing for explaining operation of an active matrix type liquid crystal display.
[Drawing 2] It is the plan to which the important section of a TFT array substrate was expanded.
[Drawing 3] It is a cross section explaining the manufacture method of the TFT array substrate of drawing 2 by the Prior art.
[Drawing 4] It is a cross section explaining the manufacture method of the TFT array substrate of drawing 2 by the Prior art, and is drawing showing the process which follows drawing 3 .
[Drawing 5] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 1 of operation of this invention.
[Drawing 6] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 1 of operation of this invention, and is drawing showing the process which follows drawing 5 .
[Drawing 7] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 1 of operation of this invention, and is drawing showing the process which follows drawing 6 .
[Drawing 8] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 2 of operation of this invention.
[Drawing 9] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 3 of operation of this invention.
[Drawing 10] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 3 of operation of this invention, and is drawing showing the process which follows drawing 9 .
[Drawing 11] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 3 of operation of this invention, and is drawing showing the process which follows drawing 10 .
[Drawing 12] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 4 of operation of this invention.
[Drawing 13] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 4 of operation of this invention, and is drawing showing the process which follows drawing 12 .
[Drawing 14] It is a cross section explaining the manufacture method of a TFT array substrate by the gestalt 5 of operation of this invention.
[Description of Notations]
1 Gate Wiring
2 Source Wiring
7 Switching Element
8 Liquid Crystal Capacity
9 Auxiliary Capacity
12 Gate Electrode
13 Gate Wiring
14 Common Wiring
15 Lower Pad
16 Gate Insulator Layer

17 1st Semiconductor Layer
18 2nd Semiconductor Layer (Impurity Semiconductor Layer)
19 2nd Metal Layer
20 Source Wiring
21 Source Electrode
22 Drain Electrode
23 Lower Pad
24, 25, 26 Contact hole
27 Pixel Electrode
28 29 Up pad
35 Protective Coat
36 Resist Pattern
37 ITO Film

[Translation done.]

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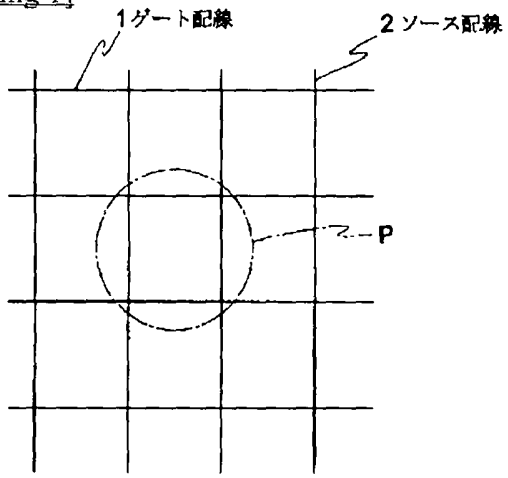
DRAWINGS

[Drawing 1]

(a)



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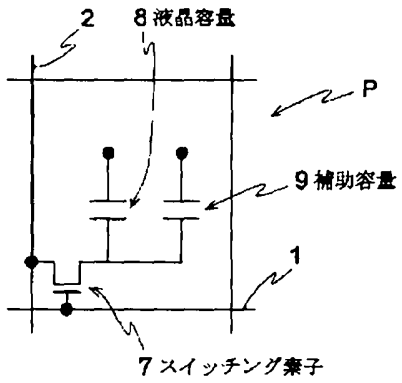
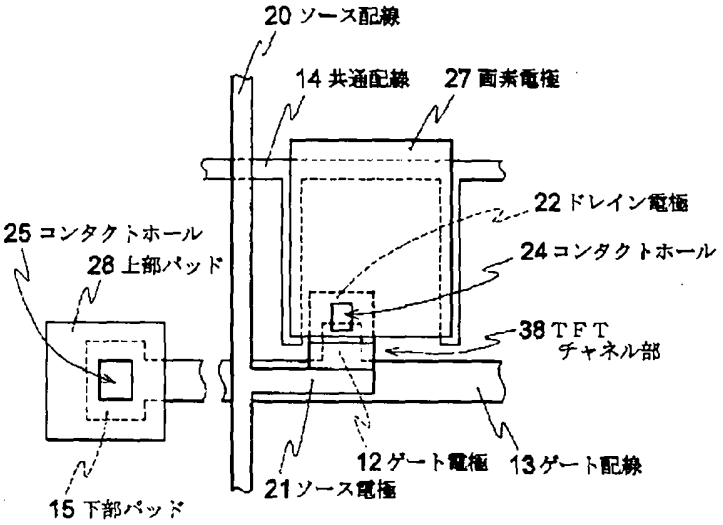
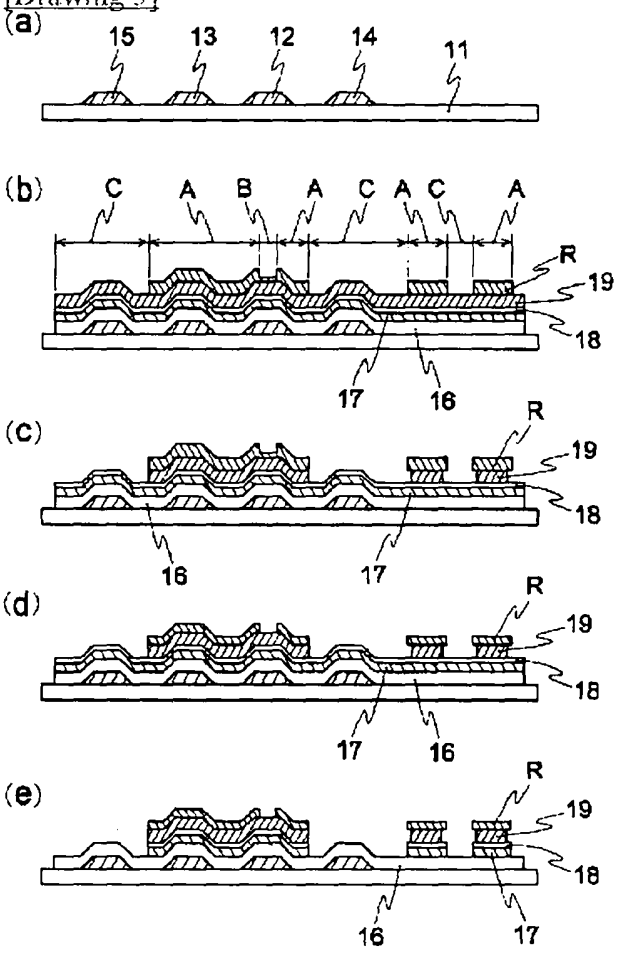


[Drawing 2]

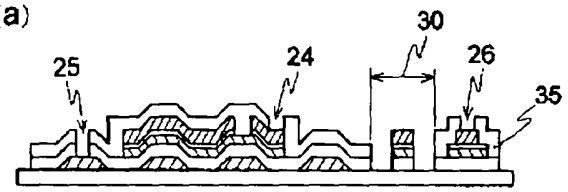


[Drawing 3]

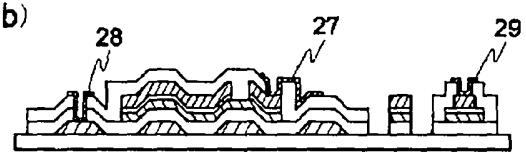


[Drawing 7]

(a)

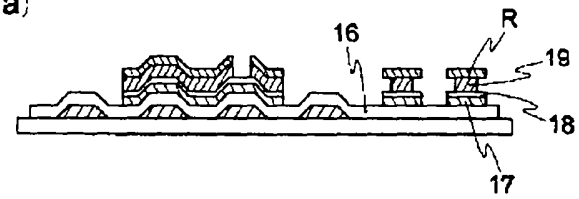


(b)



[Drawing 4]

(a)



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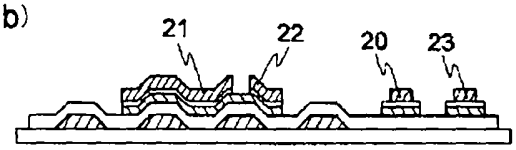
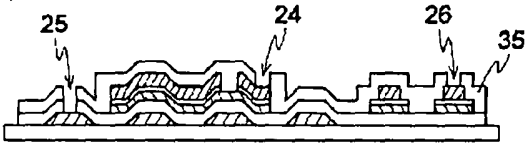
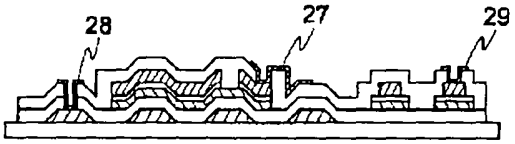


(c)



(d)



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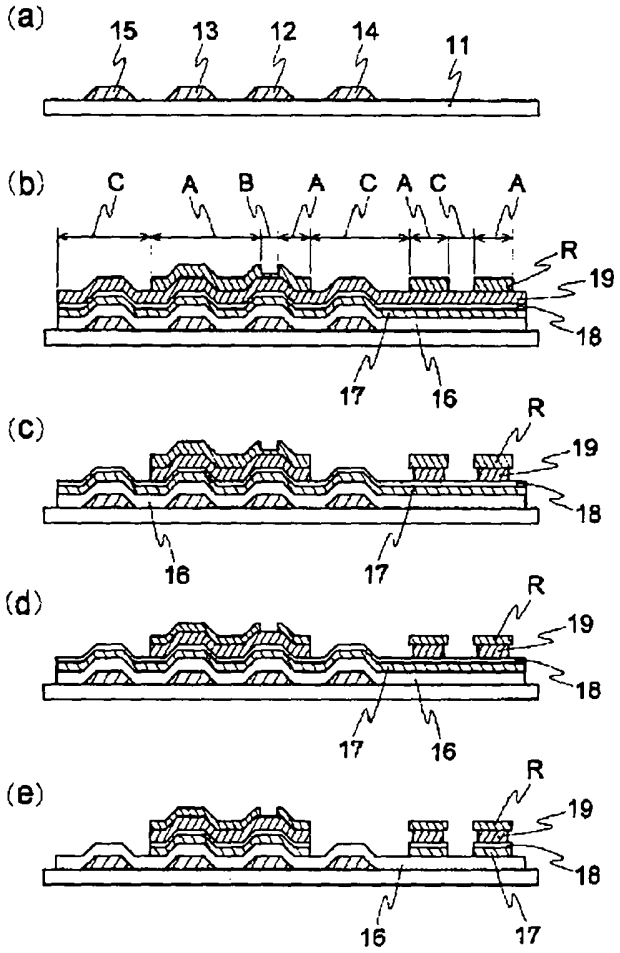
(a)
15
13
12
14
11
(b)
C
A
B
A
C
A
C
A
R
19
18
17
16
(c)
R
19
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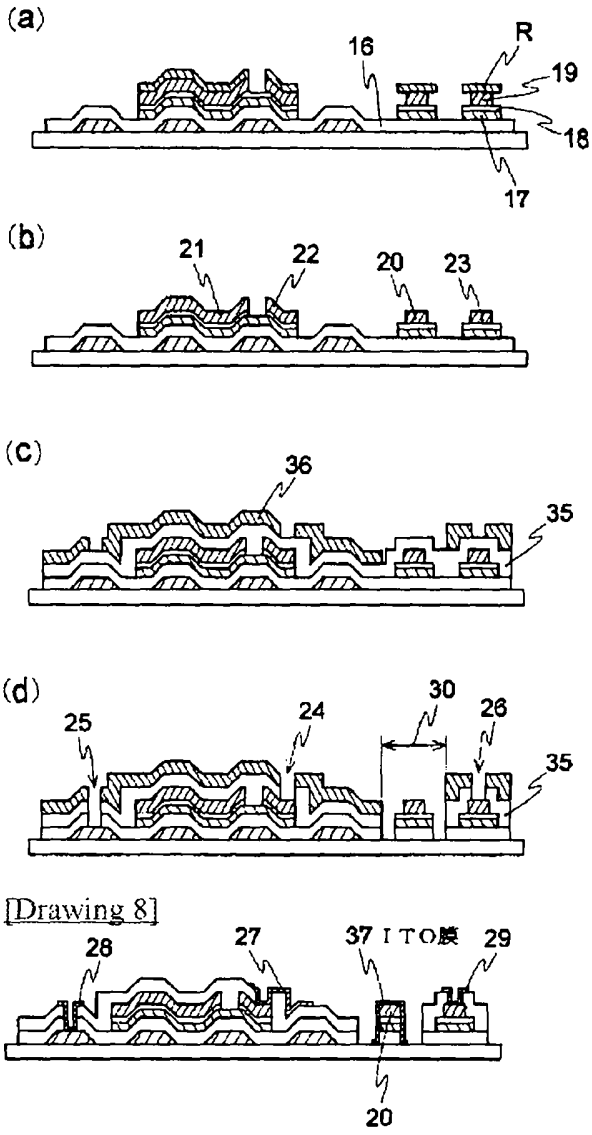
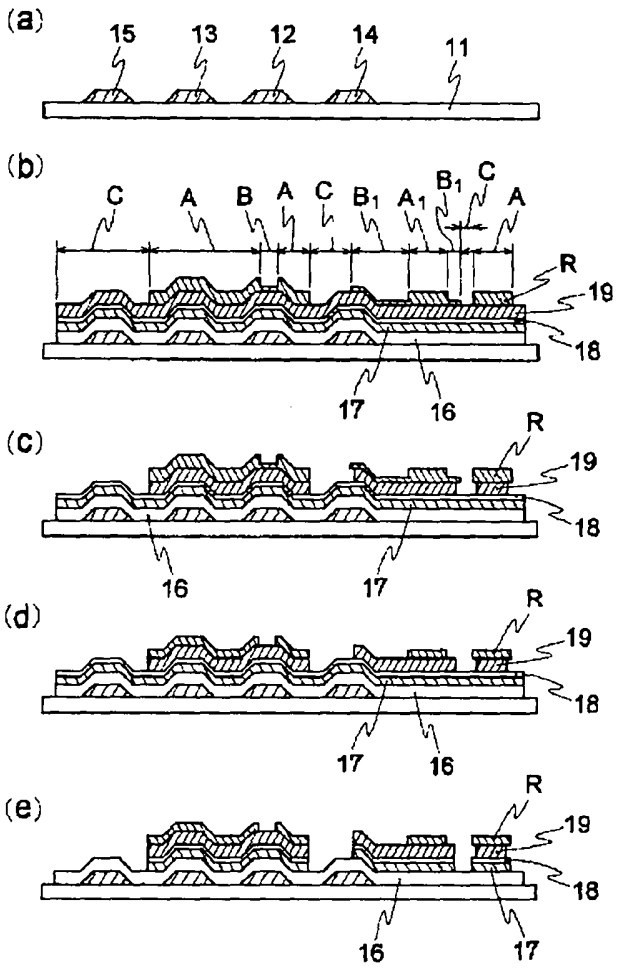
16
17
(d)
R
19
18
17
16
(e)
R
19
18
16
17

[Drawing 6]



[Drawing 8]

[Drawing 9]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12
14
11
(b)
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B
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C
B1
A1
B1
C
A
R
19
18
17
16
(c)
R
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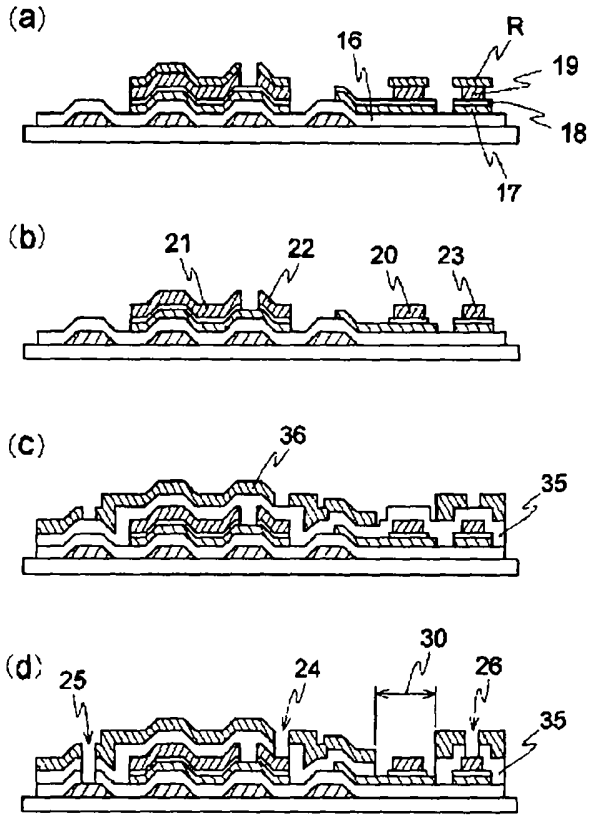
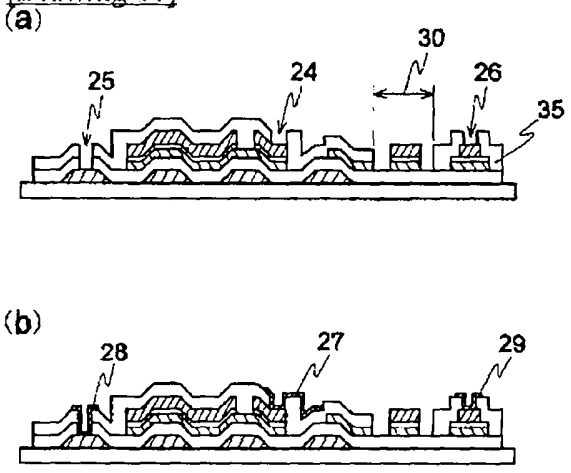
16
17
(d)
R
19
18
17
16
(e)
R
19
18
16
17

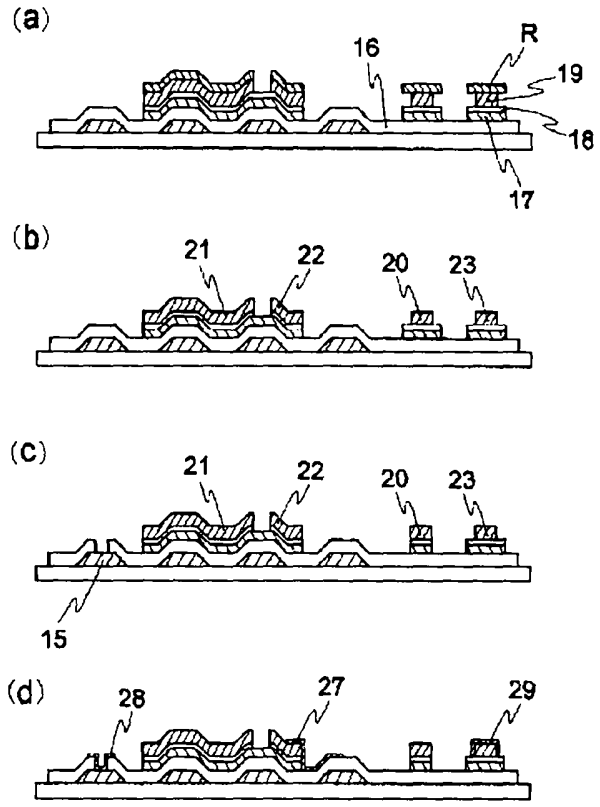
[Drawing 10]



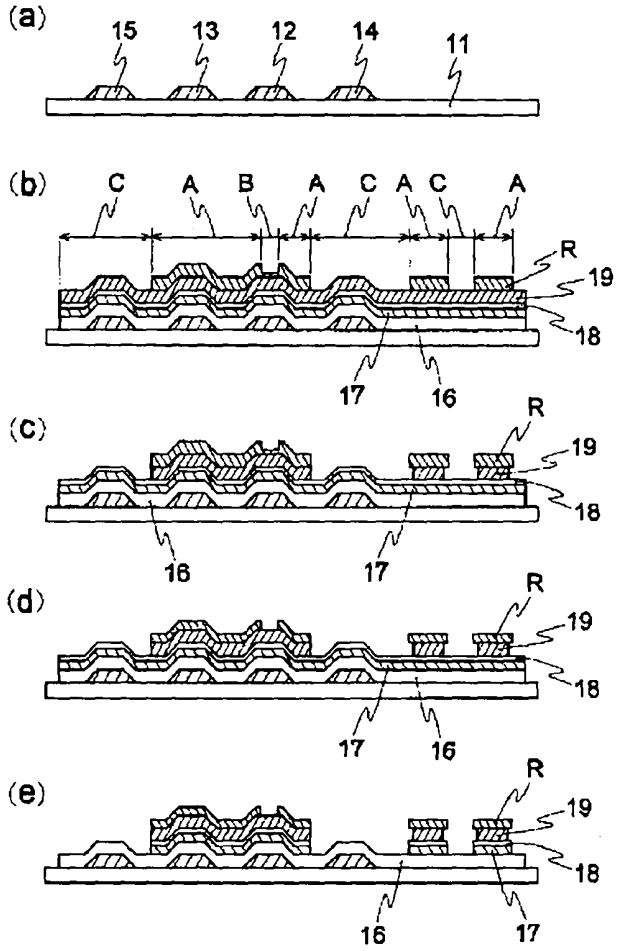
[Drawing 11]



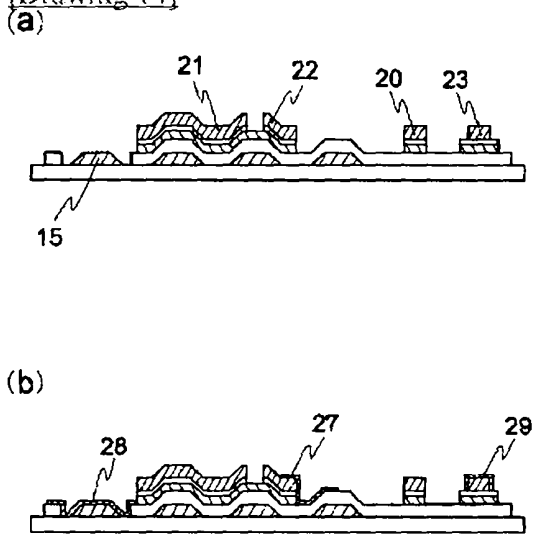
[Drawing 13]



[Drawing 12]



[Drawing 14]



[Translation done.]